

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. ARC.015A	APPLICATION NO. 09/808,469
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT Peter Warnes	
(USE SEVERAL SHEETS IF NECESSARY)		FILING DATE March 14, 2001	GROUP 2123



U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
MJ	5,463,746	10/31/95	Brodnax, et al.			
MJ	5,748,650	05/05/98	Blaker, et al.			
MJ	5,764,994	06/09/98	David John Craft			
MJ	5,794,010	08/11/98	Worrell, et al.			
MJ	5,867,681	02/02/99	Worrell, et al.			
MJ	5,896,519	04/20/99	Frank Worrell			
MJ	5,901,310	05/04/99	Rahman, et al.			
MJ	5,905,893	05/18/99	Frank Worrell			
MJ	6,195,743	02/27/01	Elmootazbellah Elnozahy			
MJ	6,233,674	05/15/01	Elmootazbellah Elnozahy			
MJ	6,237,080	05/22/01	Rauno Makinen			
MJ	6,263,429	07/17/01	Charles P. Siska			
MJ	6,268,809	07/31/01	Akira Saito			
MJ	6,275,921	08/14/01	Iwata, et al.			

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
MJ	15 Lefugry, Charles, et al. (1999) "Evaluation of a High Performance Code Compression Method," IEEE - Proceedings of Micro 32 (consisting of 10 pages).
MJ	16 Application Serial No. 09/418,663 entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design," filed October 14, 1999 - Attorney Docket No. ARC.001A

EXAMINER	DATE CONSIDERED
Mary Saito	4-19-04

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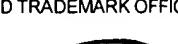
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EXAMINER 	DATE CONSIDERED <u>4-19-2004</u>
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INITIAL	REF ID	REFERENCE
<i>AN</i>	24	Berekovic, et al., (Oct. 1998), "A Core Generator for Fully Synthesizable and Highly Parameterizable RISC-Cores for System-On-Chip Designs," IEEE Workshop on Signal Processing Systems, SIPS, Design and Implementation, Pages 561-568, XP002137267
<i>AN</i>	25	Karl Guttag (March 1983), "μP's on-chip macrocode extends instruction set," Electronic Design, Vol. 31, No. 5, Pages 157-161
<i>AN</i>	26	Dolle, et al., (July 1997), "A 32-b RISC/DSP Microprocessor with Reduced Complexity," IEEE Journal of Solid-State Circuits, IEEE Inc., New York, Vol. 32, No. 7, Pages 1056-1066, XP000729365

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